AIN Templates on Silicon



Kyma AIN templates on silicon are grown using a modified plasma vapor deposition of nanocolumns process (PVDNC[™]) and provide a high quality AIN buffer for subsequent III-N device epitaxy. Kyma AIN provides customers with a nucleation layer on which power devices can be directly grown without issues associated with the Ga 'meltback' phenomenon. Kyma AIN on Si templates have several advantages over MOCVD and HVPE grown-templates which include:

- Increase in MOCVD throughput by eliminating the AIN template layer growth steps
- Lower cost and superior scalability compared to MOCVD or HVPE-derived AIN templates
- Available up to 200mm, or on Kyma or customer-provided Si at 200nm (other thicknesses available upon request)

Properties: Si/AIN Orientation: (111)/(00.1) AIN Conduction Type: Semi-insulating XRD Linewidth (002): ~1degree Front Surface Finish (Al-face): Epi-ready, RMS <2 nm (for 200nm thick AIN)



0nm

AFM of Kyma 200nm AIN on Si template